

FEATURES

- Half-duplex, isolated RS-485 transceiver
- PROFIBUS[®]-compliant
- ANSI EIA/TIA 485-A and ISO 8482: 1987(E) compliant
- 20 Mbps data rate
- 5 V or 3 V operation (V_{DD1})
- High common-mode transient immunity: >25 kV/ μ s
- Isolated DE status output
- Receiver open-circuit, fail-safe design
- Thermal shutdown protection
- 50 nodes on bus
- Safety and regulatory approvals
 - UL recognition—2500 V_{rms} for 1 minute per UL 1577
 - CSA Component Acceptance Notice #5A
 - VDE Certificate of Conformity
 - DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01
 - DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000
- $V_{IORM} = 560$ V peak
- Operating temperature range: -40°C to +85°C
- Wide body, 16-lead SOIC package

APPLICATIONS

- Isolated RS-485/RS-422 interfaces
- PROFIBUS networks
- Industrial field networks
- Multipoint data transmission systems

GENERAL DESCRIPTION

The ADM2486 differential bus transceiver is an integrated, galvanically isolated component designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and complies with ANSI EIA/TIA-485-A and ISO 8482: 1987(E).



Rev. C

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FUNCTIONAL BLOCK DIAGRAM

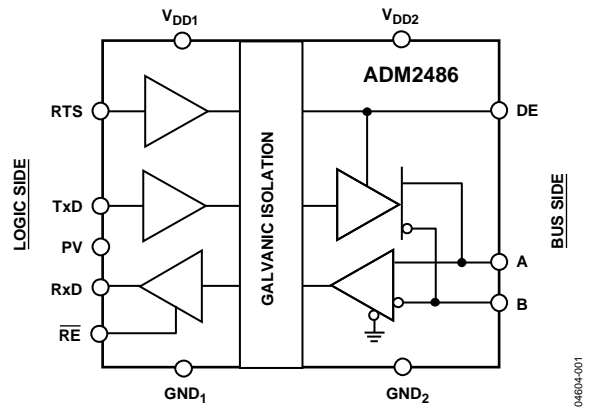


Figure 1.

The device employs Analog Devices' *iCoupler* technology to combine a 3-channel isolator, a three-state differential line driver, and a differential input receiver into a single package. The logic side of the device is powered with either a 5 V or a 3 V supply, and the bus side uses an isolated 5 V supply.

The ADM2486 driver has an active-high enable feature. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output port that imposes minimal loading on the bus when the driver is disabled or when V_{DD1} or $V_{DD2} = 0$ V. Also provided is an active-high receiver disable feature that causes the receive output to enter a high impedance state.

The device has current-limiting and thermal shutdown features to protect against output short circuits and situations where bus contention might cause excessive power dissipation. The part is fully specified over the industrial temperature range and is available in a 16-lead, wide body SOIC package.

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REVISION HISTORY**3/05—Rev. B to Rev. C**

Change to Package Characteristics.....	7
Changes to Figure 12, Figure 14, and Figure 15	11
Change to Power_Valid Input Section.....	16

1/05—Rev. A to Rev. B

Added PROFIBUS logo	1
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11/04—Rev. 0 to Rev. A

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SPECIFICATIONS

$2.7\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $4.75\text{ V} \leq V_{DD2} \leq 5.25\text{ V}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Differential Outputs					
Differential Output Voltage, V_{OD}			5	V	$R = \infty$, see Figure 3
	2.1		5	V	$R = 50\ \Omega$ (RS-422), see Figure 3
	2.1		5	V	$R = 27\ \Omega$ (RS-485), see Figure 3
	2.1		5	V	$V_{TST} = -7\text{ V}$ to 12 V , $V_{DD1} \geq 4.7$, see Figure 4
$\Delta V_{OD} $ for Complementary Output States			0.2	V	$R = 27\ \Omega$ or $50\ \Omega$, see Figure 3
Common-Mode Output Voltage, V_{OC}			3	V	$R = 27\ \Omega$ or $50\ \Omega$, see Figure 3
$\Delta V_{OC} $ for Complementary Output States			0.2	V	$R = 27\ \Omega$ or $50\ \Omega$, see Figure 3
Output Short-Circuit Current, $V_{OUT} = \text{High}$	60		200	mA	$-7\text{ V} \leq V_{OUT} \leq +12\text{ V}$
Output Short-Circuit Current, $V_{OUT} = \text{Low}$	60		200	mA	$-7\text{ V} \leq V_{OUT} \leq +12\text{ V}$
Bus Enable Output					
Output High Voltage	$V_{DD2} - 0.1$			V	$I_{ODE} = 20\ \mu\text{A}$
	$V_{DD2} - 0.3$	$V_{DD2} - 0.1$		V	$I_{ODE} = 1.6\text{ mA}$
	$V_{DD2} - 0.4$	$V_{DD2} - 0.2$		V	$I_{ODE} = 4\text{ mA}$
Output Low Voltage			0.1	V	$I_{ODE} = -20\ \mu\text{A}$
		0.1	0.3	V	$I_{ODE} = -1.6\text{ mA}$
		0.2	0.4	V	$I_{ODE} = -4\text{ mA}$
Logic Inputs					
Input High Voltage	$0.7 V_{DD1}$			V	TxD, RTS, $\overline{\text{RE}}$, PV
Input Low Voltage			$0.25 V_{DD1}$	V	TxD, RTS, $\overline{\text{RE}}$, PV
CMOS Logic Input Current (TxD, RTS, $\overline{\text{RE}}$, PV)	-10	0.01	10	μA	TxD, RTS, $\overline{\text{RE}}$, PV = V_{DD1} or 0 V
RECEIVER					
Differential Inputs					
Differential Input Threshold Voltage, V_{TH}	-200		200	mV	$-7\text{ V} \leq V_{CM} \leq +12\text{ V}$
Input Hysteresis		70		mV	$-7\text{ V} \leq V_{CM} \leq +12\text{ V}$
Input Resistance (A, B)	20	30		k Ω	$-7\text{ V} \leq V_{CM} \leq +12\text{ V}$
Input Current (A, B)			0.6	mA	$V_{IN} = +12\text{ V}$
			-0.35	mA	$V_{IN} = -7\text{ V}$
RxD Logic Output					
Output High Voltage	$V_{DD1} - 0.1$			V	$I_{OUT} = 20\ \mu\text{A}$, $V_A - V_B = 0.2\text{ V}$
	$V_{DD1} - 0.4$	$V_{DD1} - 0.2$		V	$I_{OUT} = 4\text{ mA}$, $V_A - V_B = 0.2\text{ V}$
Output Low Voltage			0.1	V	$I_{OUT} = -20\ \mu\text{A}$, $V_A - V_B = -0.2\text{ V}$
		0.2	0.4	V	$I_{OUT} = -4\text{ mA}$, $V_A - V_B = -0.2\text{ V}$
Output Short-Circuit Current	7		85	mA	$V_{OUT} = \text{GND}$ or V_{CC}
Three-State Output Leakage Current			± 1	μA	$0.4\text{ V} \leq V_{OUT} \leq 2.4\text{ V}$

ADM2486

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY CURRENT					
Logic Side		2.9	1.3	mA	RTS = 0 V, V _{DD1} = 5.5 V
		10.2		mA	2 Mbps, V _{DD1} = 5.5 V, see Figure 5
				mA	20 Mbps, V _{DD1} = 5.5 V, see Figure 5
			0.8	mA	RTS = 0 V, V _{DD1} = 3 V
			1.1	mA	2 Mbps, V _{DD1} = 3 V, see Figure 5
		4.3		mA	20 Mbps, V _{DD1} = 3 V, see Figure 5
Bus Side			3.0	mA	RTS = 0 V
		53.4		mA	2 Mbps, RTS = V _{DD1} , see Figure 5
		86.7		mA	20 Mbps, RTS = V _{DD1} , see Figure 5
COMMON-MODE TRANSIENT IMMUNITY ¹	25			kV/μs	V _{CM} = 1 kV, transient magnitude = 800 V
HIGH FREQUENCY, COMMON-MODE NOISE IMMUNITY		100		mV	V _{HF} = +5 V, -2 V < V _{TEST2} < 7 V, 1 MHz < f _{TEST} < 50 MHz, see Figure 6

¹ Common-mode transient immunity is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common-mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS

$2.7\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $4.75\text{ V} \leq V_{DD2} \leq 5.25\text{ V}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Maximum Data Rate	20			Mbps	
Propagation Delay, t_{PLH} , t_{PHL}	25	45	55	ns	$R_{LDIFF} = 54\ \Omega$, $C_{L1} = C_{L2} = 100\text{ pF}$, see Figure 7
RTS-to-DE Propagation Delay	20	35	55	ns	See Figure 8
Pulse Width Distortion, t_{PWD}			5	ns	$R_{LDIFF} = 54\ \Omega$, $C_{L1} = C_{L2} = 100\text{ pF}$, see Figure 7 and Figure 12
Switching Skew, t_{SKEW}		2	5	ns	$R_{LDIFF} = 54\ \Omega$, $C_{L1} = C_{L2} = 100\text{ pF}$, see Figure 7 and Figure 12
Rise/Fall Time, t_R , t_F		5	15	ns	$R_{LDIFF} = 54\ \Omega$, $C_{L1} = C_{L2} = 100\text{ pF}$, see Figure 7 and Figure 12
Enable Time		43	53	ns	See Figure 9 and Figure 14
Disable Time		43	55	ns	See Figure 9 and Figure 14
Enable Skew, $ t_{AZH} - t_{BZL} $, $ t_{AZL} - t_{BZH} $		1	3	ns	See Figure 9 and Figure 14
Disable Skew, $ t_{AHZ} - t_{BLZ} $, $ t_{ALZ} - t_{BHZ} $		2	5	ns	See Figure 9 and Figure 14
RECEIVER					
Propagation Delay, t_{PLH} , t_{PHL}	25	45	55	ns	$C_L = 15\text{ pF}$, see Figure 10 and Figure 13
Differential Skew, t_{SKEW}			5	ns	$C_L = 15\text{ pF}$, see Figure 10 and Figure 13
Enable Time		3	13	ns	$R_L = 1\text{ k}\Omega$, $C_L = 15\text{ pF}$, see Figure 11 and Figure 15
Disable Time		3	13	ns	$R_L = 1\text{ k}\Omega$, $C_L = 15\text{ pF}$, see Figure 11 and Figure 15
POWER_VALID INPUT					
Enable Time		1	2	μs	
Disable Time		3	5	μs	

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted. All voltages are relative to their respective ground.

Table 3.

Parameter	Rating
V_{DD1}	-0.5 V to +7 V
V_{DD2}	-0.5 V to +6 V
Digital Input Voltage (RTS, $\overline{\text{RE}}$, TxD)	-0.5 V to $V_{DD1} + 0.5 \text{ V}$
Digital Output Voltage	
RxD	-0.5 V to $V_{DD1} + 0.5 \text{ V}$
DE	-0.5 V to $V_{DD2} + 0.5 \text{ V}$
Driver Output/Receiver Input Voltage	-9 V to +14 V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +150°C
Average Output Current per Pin	-35 mA to +35 mA
θ_{JA} Thermal Impedance	73°C/W
Lead Temperature	
Soldering (10 sec)	260°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ADM2486 CHARACTERISTICS

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-Output) ¹	R _{I-O}		10 ¹²		Ω	
Capacitance (Input-Output) ¹	C _{I-O}		3		pF	f = 1 MHz
Input Capacitance ²	C _I		4		pF	
Input IC Junction-to-Case Thermal Resistance	θ _{JCI}		33		°C/W	Thermocouple located at center of package underside
Output IC Junction-to-Case Thermal Resistance	θ _{JCO}		28		°C/W	

¹ Device considered a 2-terminal device: Pins 1, 2, 3, 4, 5, 6, 7, and 8 shorted together, and Pins 9, 10, 11, 12, 13, 14, 15, and 16 shorted together.

² Input capacitance is from any input data pin to ground

REGULATORY INFORMATION

The ADM2486 has been approved by the following organizations:

Table 5.

Organization	Approval Type	Notes
UL	Recognized under 1577 component recognition program. File E214100	In accordance with UL1577, each ADM2486 is proof tested by applying an insulation test voltage ≥3000 V rms for 1 sec (current leakage detection limit = 5 μA).
CSA	Approved under CSA Component Acceptance Notice #5A. File 205078.	
VDE	Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01 Complies with DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01, DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000 File 2471900-4880-0001	In accordance with VDE 0884, each ADM2486 is proof tested by applying an insulation test voltage ≥1050 V _{PEAK} for 1 sec (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration.
Minimum External Air Gap (Clearance)	L(I01)	7.45 min	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	8.1 min	mm	Measured from input terminals to output terminals, shortest distance along body.
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1).

ADM2486

VDE 0884 INSULATION CHARACTERISTICS

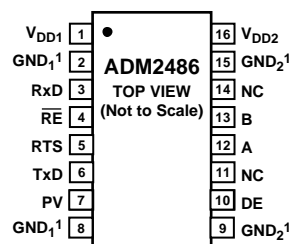
This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits.

An asterisk (*) on the physical package denotes VDE 0884 approval for 560 V peak working voltage.

Table 7.

Description	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 for Rated Mains Voltage		I to IV	
≤150 V rms		I to III	
≤300 V rms		I to II	
≤400 V rms		40/85/21	
Climatic Classification		2	
Pollution Degree (DIN VDE 0110, Table 1)		560	V _{PEAK}
Maximum Working Insulation Voltage	V _{IORM}	1050	V _{PEAK}
Input-to-Output Test Voltage, Method b1	V _{PR}		
V _{IORM} × 1.875 = V _{PR} , 100% Production Tested, t _m = 1 sec, Partial Discharge < 5 pC			
Input-to-Output Test Voltage, Method a			
(After Environmental Tests, Subgroup 1)			
V _{IORM} × 1.6 = V _{PR} , t _m = 60 sec, Partial Discharge < 5 pC		896	V _{PEAK}
(After Input and/or Safety Test, Subgroup 2/3)			
V _{IORM} × 1.2 = V _{PR} , t _m = 60 sec, Partial Discharge < 5 pC	V _{PR}	672	V _{PEAK}
Highest Allowable Overvoltage			
(Transient Overvoltage, t _{TR} = 10 sec)	V _{TR}	4000	V _{PEAK}
Safety-Limiting Values (Maximum Value Allowed in the Event of a Failure. See Figure 21.)			
Case Temperature	T _S	150	°C
Input Current	I _{S, INPUT}	265	mA
Output Current	I _{S, OUTPUT}	335	mA
Insulation Resistance at T _S , V _{IO} = 500 V	R _S	>10 ⁹	Ω

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NC = NO CONNECT

¹ PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED.
EITHER OR BOTH MAY BE USED FOR GND₁.
PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED.
EITHER OR BOTH MAY BE USED FOR GND₂.

04604-003

Figure 2. Pin Configuration

Table 8.

Pin No.	Mnemonic	Function
1	V _{DD1}	Power Supply (Logic Side).
2, 8	GND ₁	Ground (Logic Side).
3	RxD	Receiver Output Data. This output is high when (A – B) > 200 mV, and low when (A – B) < –200 mV. The output is three-stated when the receiver is disabled, that is, when \overline{RE} is driven high.
4	\overline{RE}	Receiver Enable Input. This is an active-low input. Driving this input low enables the receiver, and driving it high disables the receiver.
5	RTS	Request to Send Input. Driving this input high enables the driver, and driving it low disables the driver.
6	TxD	Transmit Data Input. Data to be transmitted by the driver is applied to this input.
7	PV	Power_Valid. Used during power-up and power-down. See the Applications Information section.
9, 15	GND ₂	Ground (Bus Side).
10	DE	Driver Enable Status Output. This output signals the driver enable or disable status to other devices on the bus. DE is high when the driver is enabled and low when the driver is disabled.
11, 14	NC	No Connect.
12	A	Noninverting Driver Output/Receiver Input. When the driver is disabled, or when V _{DD1} or V _{DD2} is powered down, Pin A is put into a high impedance state to avoid overloading the bus.
13	B	Inverting Driver Output/Receiver Input. When the driver is disabled, or when V _{DD1} or V _{DD2} is powered down, Pin B is put into a high impedance state to avoid overloading the bus.
16	V _{DD2}	Power Supply (Bus Side).

TEST CIRCUITS

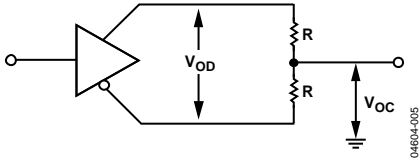


Figure 3. Driver Voltage Measurement

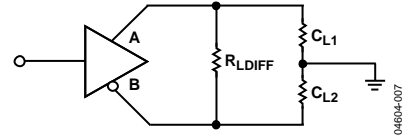


Figure 7. Driver Propagation Delay

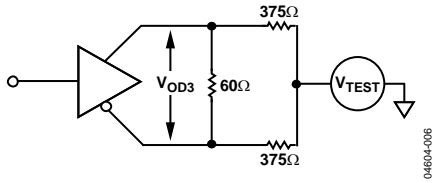


Figure 4. Driver Voltage Measurement

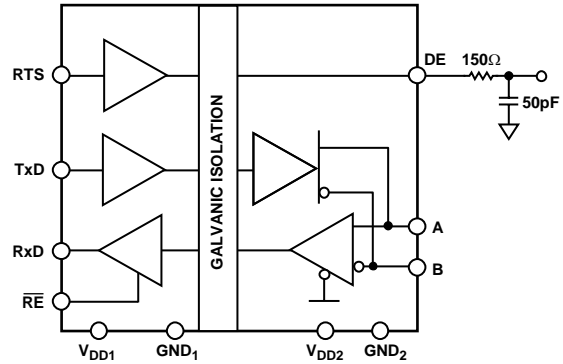


Figure 8. RTS-to-DE Propagation Delay

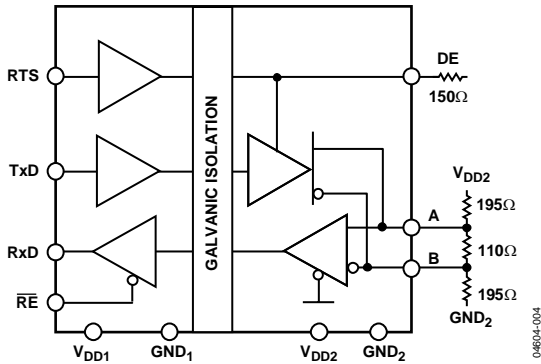


Figure 5. Supply-Current Measurement Test Circuit

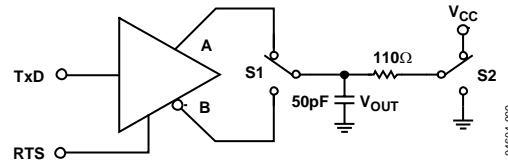


Figure 9. Driver Enable/Disable

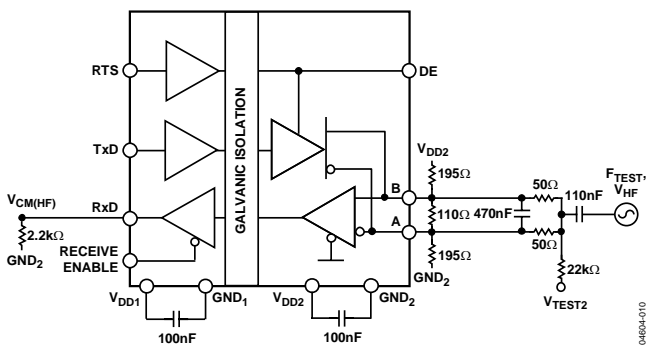


Figure 6. High Frequency Common-Mode Noise Test Circuit

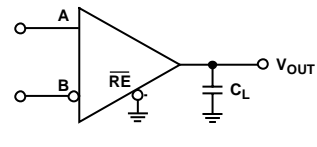


Figure 10. Receiver Propagation Delay

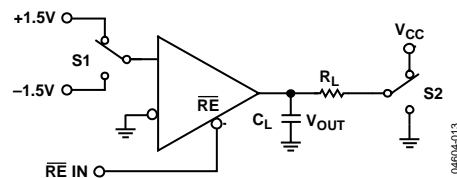


Figure 11. Receiver Enable/Disable

SWITCHING CHARACTERISTICS

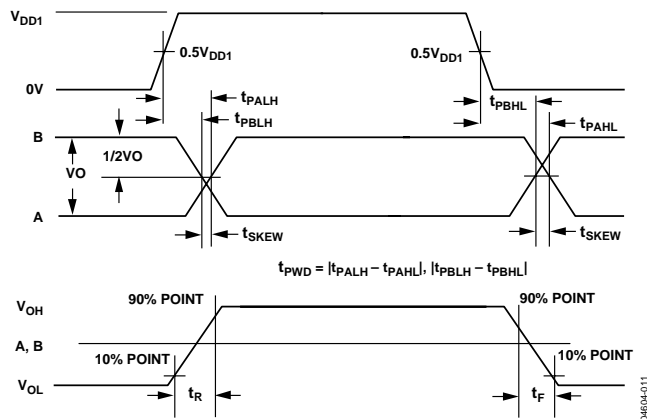


Figure 12. Driver Propagation Delay, Rise/Fall Timing

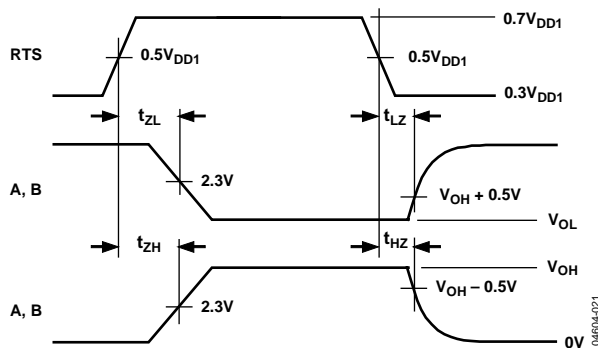


Figure 14. Driver Enable/Disable Timing

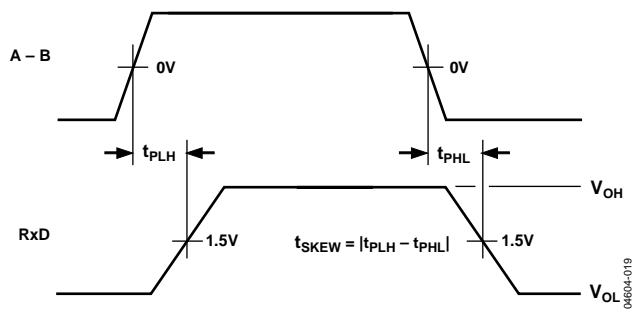


Figure 13. Receiver Propagation Delay

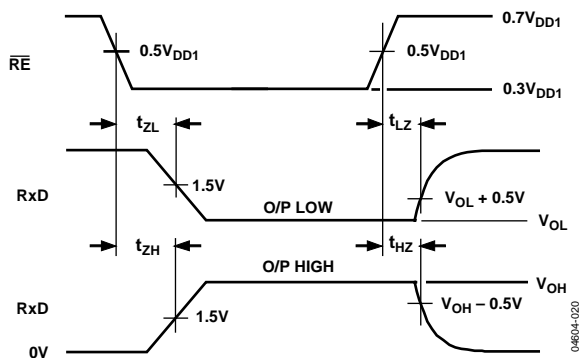


Figure 15. Receiver Enable/Disable Timing

TYPICAL PERFORMANCE CHARACTERISTICS

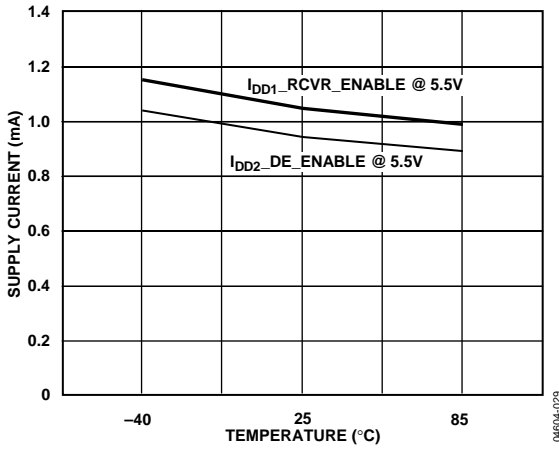


Figure 16. Unloaded Supply Current vs. Temperature

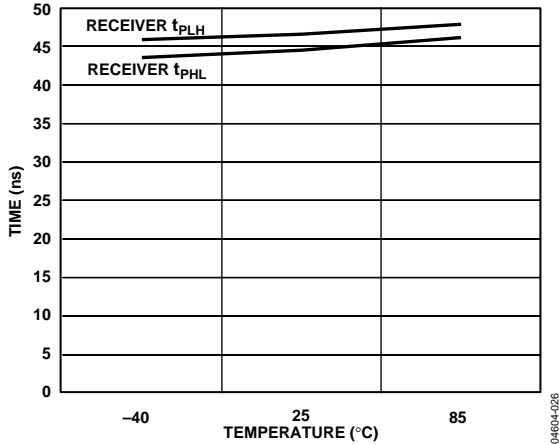


Figure 17. Driver Propagation Delay vs. Temperature

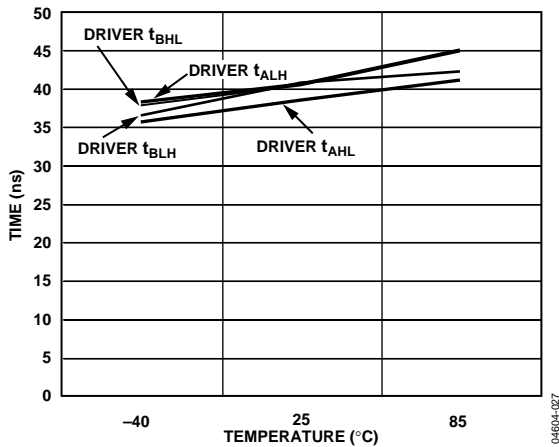


Figure 18. Receiver Propagation Delay vs. Temperature

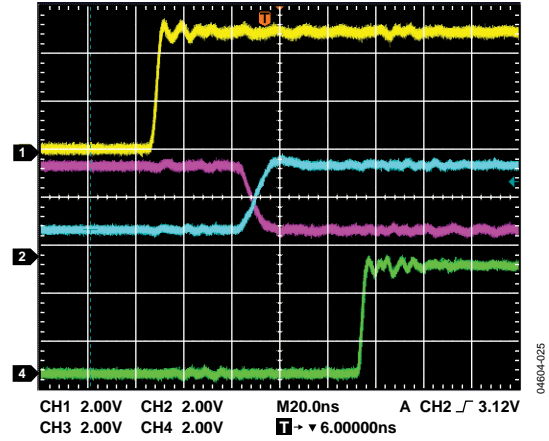


Figure 19. Driver/Receiver Propagation Delay, Low to High ($R_{LDiff} = 54 \Omega$, $C_{L1} = C_{L2} = 100 pF$)

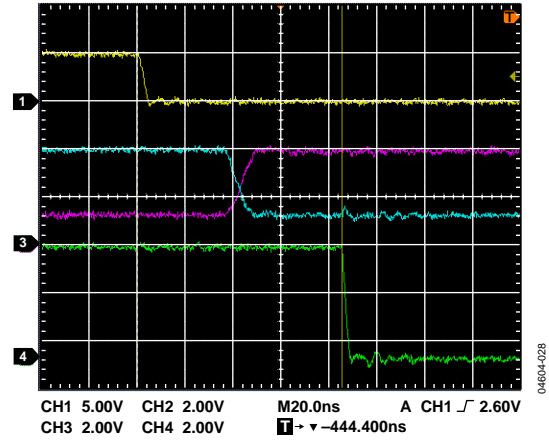


Figure 20. Driver/Receiver Propagation Delay, High to Low ($R_{LDiff} = 54 \Omega$, $C_{L1} = C_{L2} = 100 pF$)

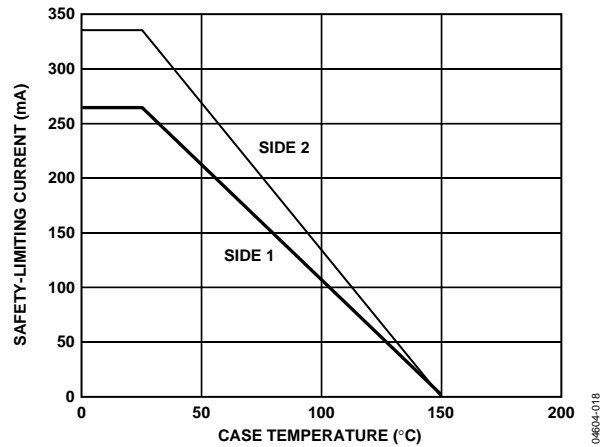


Figure 21. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per VDE 0884

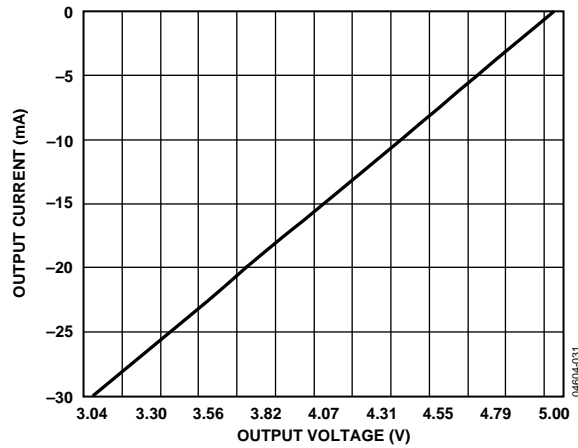


Figure 22. Output Current vs. Receiver Output High Voltage

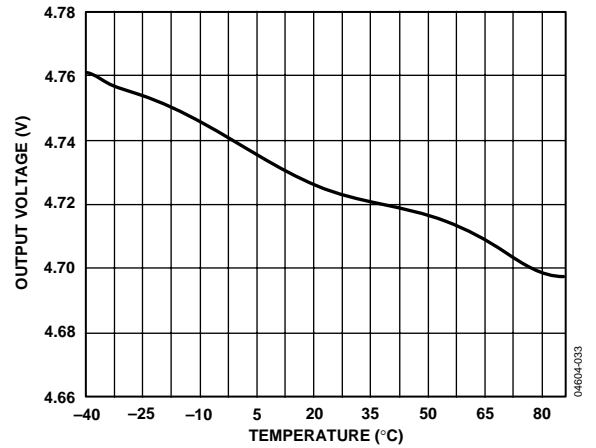


Figure 24. Receiver Output High Voltage vs. Temperature $I = -4$ mA

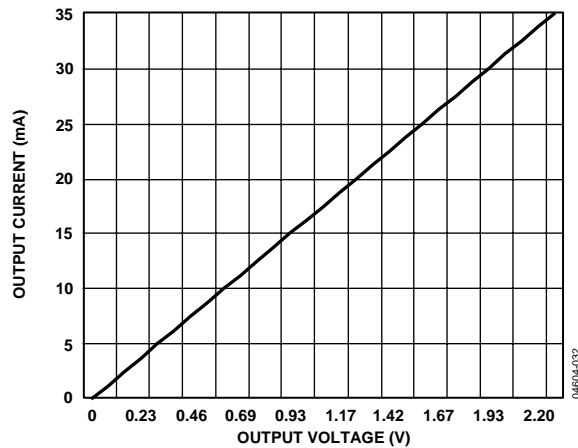


Figure 23. Output Current vs. Receiver Output Low Voltage

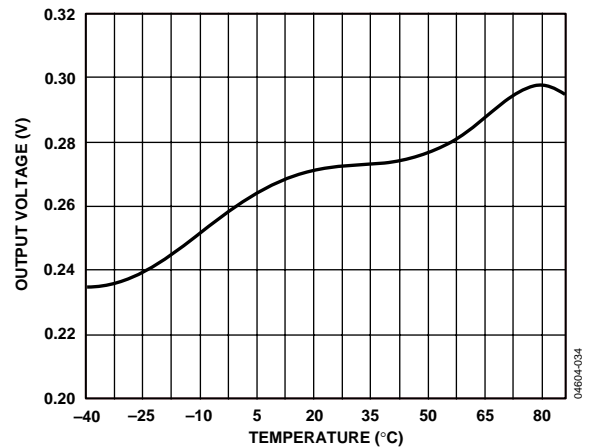


Figure 25. Receiver Output Low Voltage vs. Temperature $I = -4$ mA

CIRCUIT DESCRIPTION

ELECTRICAL ISOLATION

In the ADM2486, electrical isolation is implemented on the logic side of the interface. Therefore, the part has two main sections: a digital isolation section and a transceiver section (see Figure 26). Driver input and request-to-send signals, applied to the TxD and RTS pins, respectively, and referenced to logic ground (GND_1), are coupled across an isolation barrier to appear at the transceiver section referenced to isolated ground (GND_2). Similarly, the receiver output, referenced to isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RxD pin referenced to logic ground.

iCoupler Technology

The digital signals are transmitted across the isolation barrier using iCoupler technology. This technique uses chip-scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are then decoded into the binary value that was originally transmitted.

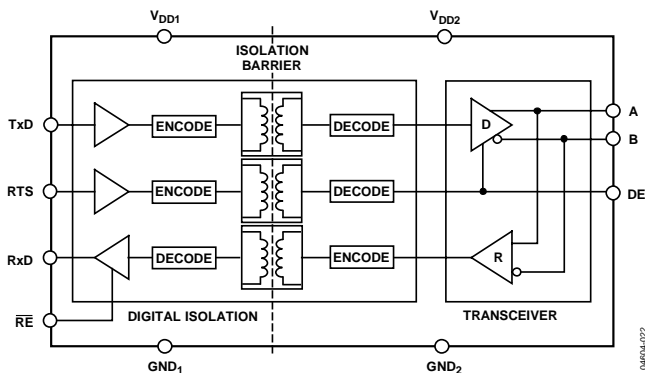


Figure 26. ADM2486 Digital Isolation and Transceiver Sections

TRUTH TABLES

The truth tables in this section use these abbreviations:

Letter	Description
H	High level
I	Indeterminate
L	Low level
X	Irrelevant
Z	High impedance (off)
NC	Disconnected

Table 9. Transmitting

Supply Status		Inputs		Output		
V _{DD1}	V _{DD2}	RTS	TxD	A	B	DE
On	On	H	H	H	L	H
On	On	H	L	L	H	H
On	On	L	X	Z	Z	L
On	Off	X	X	Z	Z	L
Off	On	X	X	Z	Z	L
Off	Off	X	X	Z	Z	L

Table 10. Receiving

Supply Status		Inputs	Output
V _{DD1}	V _{DD2}	A – B (V)	RxD
On	On	>0.2	H
On	On	<-0.2	L
On	On	-0.2 < A – B < 0.2	I
On	On	Inputs open	H
On	On	X	Z
On	Off	X	H
Off	On	X	H
Off	Off	X	L

POWER-UP/POWER-DOWN THRESHOLDS

The power-up/power-down characteristics of the ADM2486 are in accordance with the supply thresholds shown in Table 11. Upon power-up, the ADM2486 output signals (A, B, RxD, and DE) reach their correct state once both supplies have exceeded their thresholds. Upon power-down, the ADM2486 output signals retain their correct state until at least one of the supplies drops below its power-down threshold. When the V_{DD1} power-down threshold is crossed, the ADM2486 output signals reach their unpowered states within 4 μs.

Table 11. Power-Up/Power-Down Thresholds

Supply	Transition	Threshold (V)
V _{DD1}	Power-up	2.0
V _{DD1}	Power-down	1.0
V _{DD2}	Power-up	3.3
V _{DD2}	Power-down	2.4

THERMAL SHUTDOWN

The ADM2486 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at a temperature of 140°C.

RECEIVER FAIL-SAFE INPUTS

The receiver input includes a fail-safe feature that guarantees a logic high RxD output when the A and B inputs are floating or open-circuited.

MAGNETIC FIELD IMMUNITY

Because iCouplers use a coreless technology, no magnetic components are present, and the problem of magnetic saturation of the core material does not exist. Therefore, iCouplers have essentially infinite dc field immunity. The analysis below defines the conditions under which this may occur. The ADM2486's 3 V operating condition is examined because it represents the most susceptible mode of operation.

The limitation on the iCoupler's ac magnetic field immunity is set by the condition in which the induced error voltage in the receiving coil (the bottom coil in this case) is made sufficiently large, either to falsely set or reset the decoder. The voltage induced across the bottom coil is given by

$$V = \left(\frac{-d\beta}{dt} \right) \sum \pi r_n^2 ; n = 1, 2, \dots, N$$

where, if the pulses at the transformer output are greater than 1.0 V in amplitude:

- β = magnetic flux density (gauss)
- N = number of turns in receiving coil
- r_n = radius of nth turn in receiving coil (cm)

The decoder has a sensing threshold of about 0.5 V; therefore, there is a 0.5 V margin in which induced voltages can be tolerated.

Given the geometry of the receiving coil and an imposed requirement that the induced voltage is, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 27.

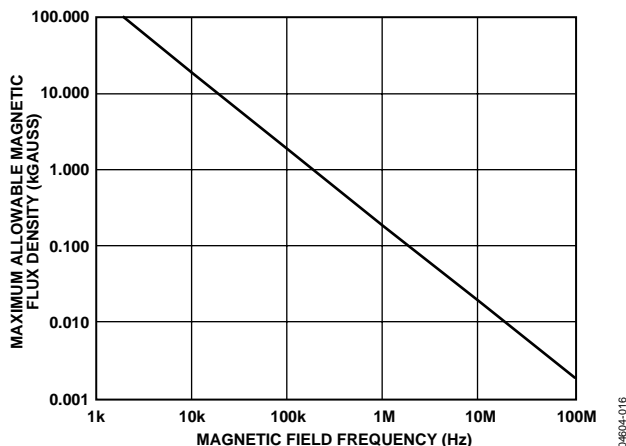


Figure 27. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kGauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse and is the worst-case polarity, it reduces the received pulse from >1.0 V to 0.75 V. This is well above the 0.5 V sensing threshold of the decoder.

Figure 28 shows the magnetic flux density values in terms of more familiar quantities such as maximum allowable current flow at given distances away from the ADM2486 transformers.

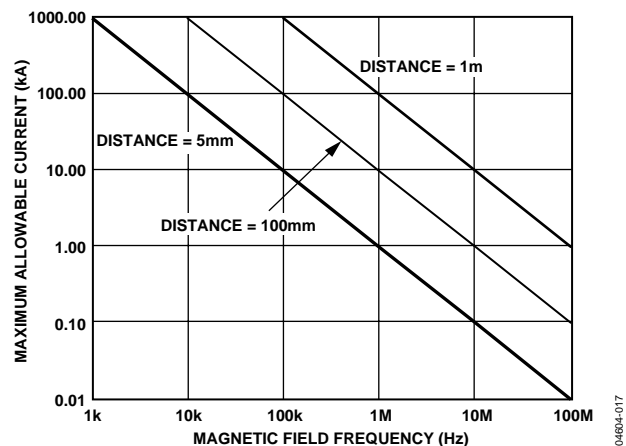


Figure 28. Maximum Allowable Current for Various Current-to-ADM2486 Spacings

At combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

APPLICATIONS INFORMATION

POWER_VALID INPUT

To avoid chatter on the A and B outputs caused by slow power-up and power-down transients on V_{DD1} ($>100 \mu\text{s/V}$), the device features a power_valid (PV) digital input. This pin should be driven low until V_{DD1} exceeds 2.0 V. When V_{DD1} is greater than 2.0 V, this pin should be driven high. Conversely, upon power-down, PV should be driven low before V_{DD1} reaches 2.0 V.

If the PV pin is driven with an open-drain output, the recommended value for the pull-up resistor is a 10 k Ω resistor, bypassed with a 100 pF capacitor to GND_1 (see Figure 30).

The power_valid input can be driven, for example, by the output of a system reset circuit such as the ADM809Z, which has a threshold voltage of 2.32 V.

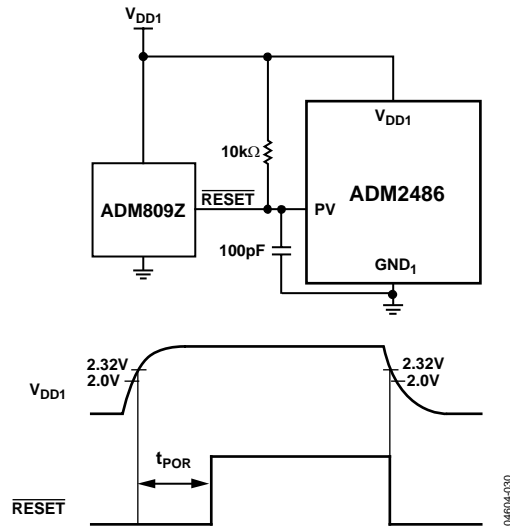


Figure 30. Driving PV with an Open-Drain Output

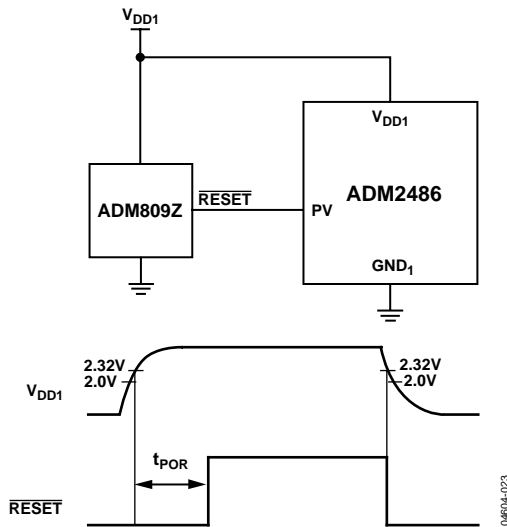


Figure 29. Driving PV with ADM809Z

ISOLATED POWER SUPPLY CIRCUIT

The ADM2486 requires isolated power capable of 5 V at 100 mA to be supplied between the V_{DD2} and GND_2 pins. If no suitable integrated power supply is available, a discrete circuit, such as the one in Figure 31, can be used. A center-tapped transformer provides electrical isolation. The primary winding is excited with a pair of square waveforms that are 180° out of phase with each other. A pair of Schottky diodes and a smoothing capacitor are used to create a rectified signal from the secondary winding. The ADP667 linear voltage regulator provides a regulated power supply to the ADM2486's bus-side circuitry.

To create the pair of square waves, a D-type flip-flop with complementary Q/\bar{Q} outputs is used. The flip-flop can be connected so that output Q follows the clock input signal. If no local clock signal is available, a simple digital oscillator can be implemented with a hex-inverting Schmitt trigger and a resistor and capacitor. In this case, values of 3.9 kΩ and 1 nF generate a 364 kHz square wave. A pair of discrete NMOS transistors, switched by the Q/\bar{Q} flip-flop outputs, conduct current through the center tap of the primary transformer, winding in an alternating fashion.

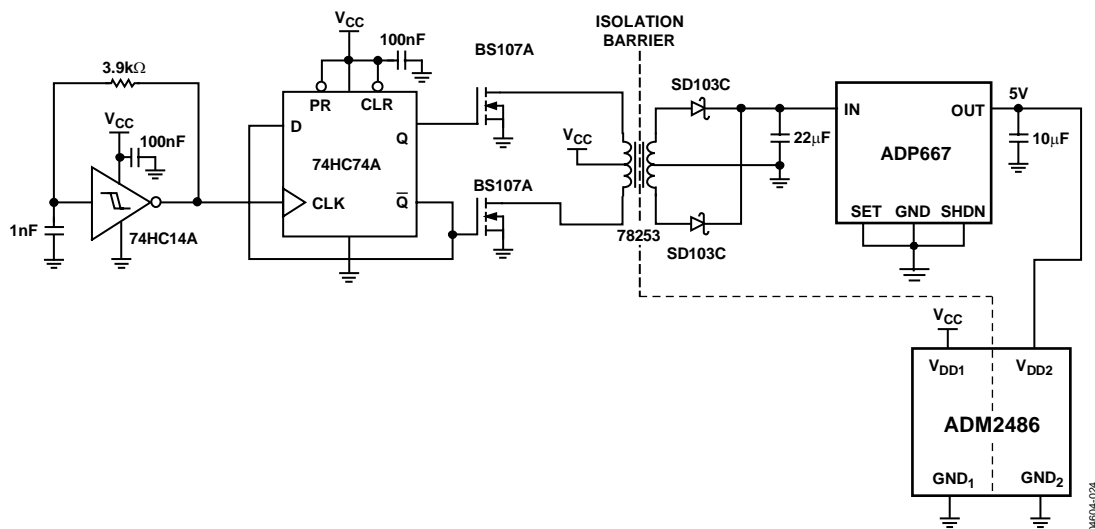
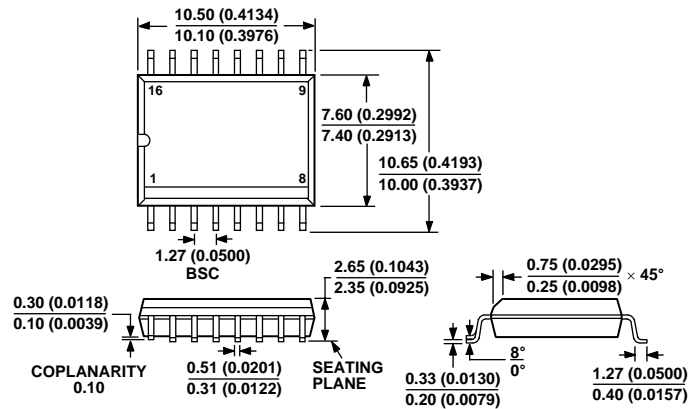


Figure 31. Isolated Power Supply Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 32. 16-Lead Standard Small Outline Package [SOIC]
 Wide Body
 (RW-16)
 Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Data Rate (Mbps)	Temperature Range	Package Description	Quantity	Package Option
ADM2486BRW	20	-40°C to +85°C	16-Lead, Wide Body SOIC	47	RW-16
ADM2486BRW-REEL	20	-40°C to +85°C	16-Lead, Wide Body SOIC	1,000	RW-16
ADM2486BRWZ ¹	20	-40°C to +85°C	16-Lead, Wide Body SOIC	47	RW-16
ADM2486BRWZ-REEL ¹	20	-40°C to +85°C	16-Lead, Wide Body SOIC	1,000	RW-16

¹ Z = Pb-free part.

NOTES

ADM2486

NOTES